IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

Claims 1-3 (canceled).

4. (previously presented) A packet switch connected to a plurality of input lines and output lines for forwarding variable length packets received from each of said input lines to one of said output lines specified by respective header information, said packet switch comprising:

a switch unit, having a plurality of input ports and output ports corresponding to said input lines and output lines, respectively, which outputs fixed length cells received from each of said input ports to one of said output ports specified by routing information contained in the cell header of said received cells;

a plurality of input line interfaces, each connected to one of said input ports, which convert the variable length packets received from one of said input lines to fixed length cells and supply the fixed length cells to the one input port; and

a plurality of output line interfaces, each connected to one of said output ports which convert output cells received from the one output port to variable length packets and send out the packets to one of said output lines,

wherein each of said input line interfaces has a cell output controller which stores the cells converted from said variable length packets in queues formed for each output line according to a degree of priority of respective cells and selectively

forwards the stored cells to said input port according to the degree of priority of the respective cells,

wherein each output line interface comprises:

a cell disassembler unit which receives the output cells from one of said output ports and delivers data blocks obtained by removing a cell header from each of said output cells,

a buffer memory connected to said cell disassembler unit,

a memory controller which stores said data blocks delivered from said disassembler into said buffer memory according to identification information contained in said cell header, and

a buffer monitor coupled with said memory controller so as to monitor the data blocks stored in said buffer memory and issue a notice of congestion indicating the cell congestion status, and

wherein the cell output controller in each of said input line interfaces selectively prohibits the forwarding of cells according to the degree of priority of the respective cells as to the output lines specified by the notice of congestion.

5. (previously presented) A packet switch according to Claim 4, further comprising:

a circuit connected to receive the notice of congestion from said output line interfaces and distribute the notice of congestion to said input line interfaces.

6. (currently amended)A packet switch connected to a plurality of input lines and output lines for forwarding variable length packets received from each of

said input lines to one of said output lines specified by respective header information, said packet switch comprising:

a switch unit, having a plurality of input ports and output ports corresponding to said input lines and output lines, respectively, which outputs fixed length cells received from each of said input ports to one of said output ports specified by routing information contained in the cell header of said received cells;

a plurality of input line interfaces, each connected to one of said input ports, which convert the variable length packets received from one of said input lines to fixed length cells and supply the fixed length cells to the one input port; and

a plurality of output line interfaces, each connected to one of said output ports which convert output cells received from the one output port to variable length packets and send out the packets to one of said output lines,

wherein each of said input line interfaces has a cell output controller which stores the cells converted from said variable length packets in queues formed for each output line according to a degree of priority of respective cells and selectively forwards the stored cells to said input port according to the degree of priority of the respective cells,

wherein each output line interface comprises:

a cell disassembler unit which delivers data blocks by removing a cell header from each of said output cells received from one of said output ports,

a buffer memory connected to receive said data blocks from said cell disassembler unit,

a memory controller which stores the data blocks into said buffer memory forming a plurality of queues according to identification information contained in the cell header, and

a buffer monitor coupled with said memory controller to monitor the quantity of data blocks stored in said buffer memory,

wherein said packet switch comprises:

a circuit which collects information indicating the quantity of stored cells from each of said output line interfaces and converts the quantity information into control information indicating the congestion status for each output line to notify said input line interfaces of the control information, and

wherein the cell output controller of each of said input line interfaces selectively prohibits the forwarding of cells according to the degree of priority of the respective cells as to the output lines specified by a notice of congestion.

7. (previously presented) A packet switch according to Claim 4, wherein said notice of congestion includes information indicating degree of congestion for each output line, and said cell output controller determines cell queues to be prohibited from cell forwarding based on the degree of congestion.

8. (previously presented) A packet switch according to Claim 4, wherein said cell output controller determines the degree of priority based on service class information contained in the header of said variable length packet.

9. (previously presented) A packet switch coupled to a first group of input lines and output lines for communicating variable length packets, and a second group of input lines and output lines for communicating fixed length cells each having a cell header and a fixed length data block obtained by segmenting a variable length packet, said packet switch comprising:

a switching unit having a plurality of input and output ports which switches the fixed length cells received from said input ports to one of said output ports specified by routing information contained in the cell header of said received cells;

a plurality of first input line interfaces which converts the variable length packets received from said first group of input lines into internal cells of a fixed length and. supply the internal cells to a first group of the input ports of said switching unit;

a plurality of second input line interfaces which converts the fixed length cells received from said second group of input lines by header conversion into internal cells of a fixed length and supply the internal cells to a second group of the input ports of said switching unit;

a plurality of first output line interfaces which converts the internal cells received from a first group of output ports of said switching unit into variable length packets and forward the variable length packets to said first group of output lines; and

a plurality of second output line interfaces which converts the internal cells received from a second group of output ports into external cells by removing a portion of the cell header from said internal cells and forward the external cells to said second group of output lines,

wherein each of said first and said second input line interfaces having a cell output controller which stores the internal cells by classifying into a plurality of queues corresponding to said output lines and selectively output the stored cells to the input port according to the degree of priority of the stored cells.

10. (previously presented) A packet switch according to Claim 9 further comprising:

a monitor which detects congestion status of stored cells for each of said output lines within said packet switch and notify the congestion status to said first and said second input line interfaces, whereby said cell output controller selectively prohibits the forwarding of stored cells as to the output lines specified by the notice of congestion.

11. (previously presented) A packet switch according to Claim 9, wherein said switch unit comprises a buffer memory for storing the input cells received from said input ports by classifying for each of said output lines, and a buffer monitor which monitors the quantity of stored cells for each of said output lines within said buffer memory and to issue a notice of congestion indicating the congestion status for each of said output lines; and

each of said cell output controllers in said first and second input line interfaces selectively prohibits the forwarding of stored cells as to the output lines specified by the notice of congestion, according to degree of priority of said stored cells.

12. (previously presented) A packet switch according to Claim 9, wherein each of said first output line interfaces comprises a circuit to output data blocks obtained by removing the cell header from the internal cells received from one of said output ports, a buffer memory to store the data blocks into queues formed according to cell identification information contained in the cell headers associated with the respective data blocks, and a buffer monitor which monitors the quantity of stored data blocks within said buffer memory and issue a notice of congestion indicating the status of congestion, and

wherein each output controller in said first and second input line interfaces selectively prohibit the forwarding of cells as to output lines specified by the notice of congestion, according to the degree of priority of said stored cells.

Claims 13 and 14 (canceled).

15. (currently amended)A packet switch ~~according to claim 3~~, connected to a plurality of input lines and output lines for forwarding variable length packets received from each of said input lines to one of said output lines specified by respective header information, said packet switch comprising:

a switch unit, having a plurality of input ports and output ports corresponding to said input lines and output lines, respectively, which outputs fixed length cells received from each of said input ports to one of said output ports specified by routing information contained in the cell header of said received cells;

a plurality of input line interfaces, each connected to one of said input ports, which convert the variable length packets received from one of said input lines to fixed length cells and supply the fixed length cells to the one input port; and

a plurality of output line interfaces, each connected to one of said output ports which convert output cells received from the one output port to variable length packets and send out the packets to one of said output lines,

wherein each of said input line interfaces has a cell output controller which stores the cells converted from said variable length packets in queues formed for each output line according to a degree of priority of respective cells and selectively forwards the stored cells to said input port according to the degree of priority of the respective cells,

wherein said switch unit comprises:

a buffer memory to store the input cells from said input ports in queues formed corresponding to said output lines, and

a buffer monitor which monitors the quantity of stored cells for each of said output lines within said queues and to issue a notice of congestion indicating the congestion status for each of said output lines,

wherein said cell output controller of each of said input line interfaces selectively prohibits the cell forwarding according to the degree of priority of the respective cells as to the output lines specified by the notice of congestion, and

wherein said notice of congestion for each output line, and said cell output controller determines cell queues to be prohibited from cell forwarding based on ~~the~~ a degree of congestion.

16. (previously presented) A packet switch according to claim 3, wherein said cell output controller determines the degree of priority based on service class information contained in the header of said variable length packet.